AT4SLC+

CPU Manual

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1.1 PRODUCT OVERVIEW

The AT4SLC+ CPU board is based on a 486SLC processor. This highly integrated, eight-layer board supports up to 16 Mbytes of fast page mode interleave DRAM, and provides an integrated floppy disk drive controller that supports up to two floppy disk drives. It also offers a high-performance, cost-effective integrated drive electronics (IDE) hard disk interface, two serial ports, one parallel port, and a VGA controller with flat panel support.

1.2 FEATURES OF THE AT4SLC+ CPU BOARD

- CPU
  - 486SLC @ 25 MHz
  - Four SIMM sites support up to 16 Mbytes of parity-checked DRAM
  - Real time clock with on-board battery backup
  - Socket for optional 80387SX or compatible math co-processor
  - Keyboard port
  - Speaker jack on ORB
  - 8.33 MHz AT bus speed
  - 1 Kbyte internal cache

- I/O Controller
  - IDE hard disk interface (supports two drives)
  - SA450 floppy disk interface (supports two drives)
  - Two 16550-compatible RS-232C serial ports
  - One Centronics-compatible parallel port

- Video Controller
  - VGA analog output
  - 512 Kbyte Super VGA support
  - Flat panel driver circuitry

1.3 OPERATIONAL DESCRIPTION

The AT4SLC+ block diagram is illustrated in Figure 1-1, below:

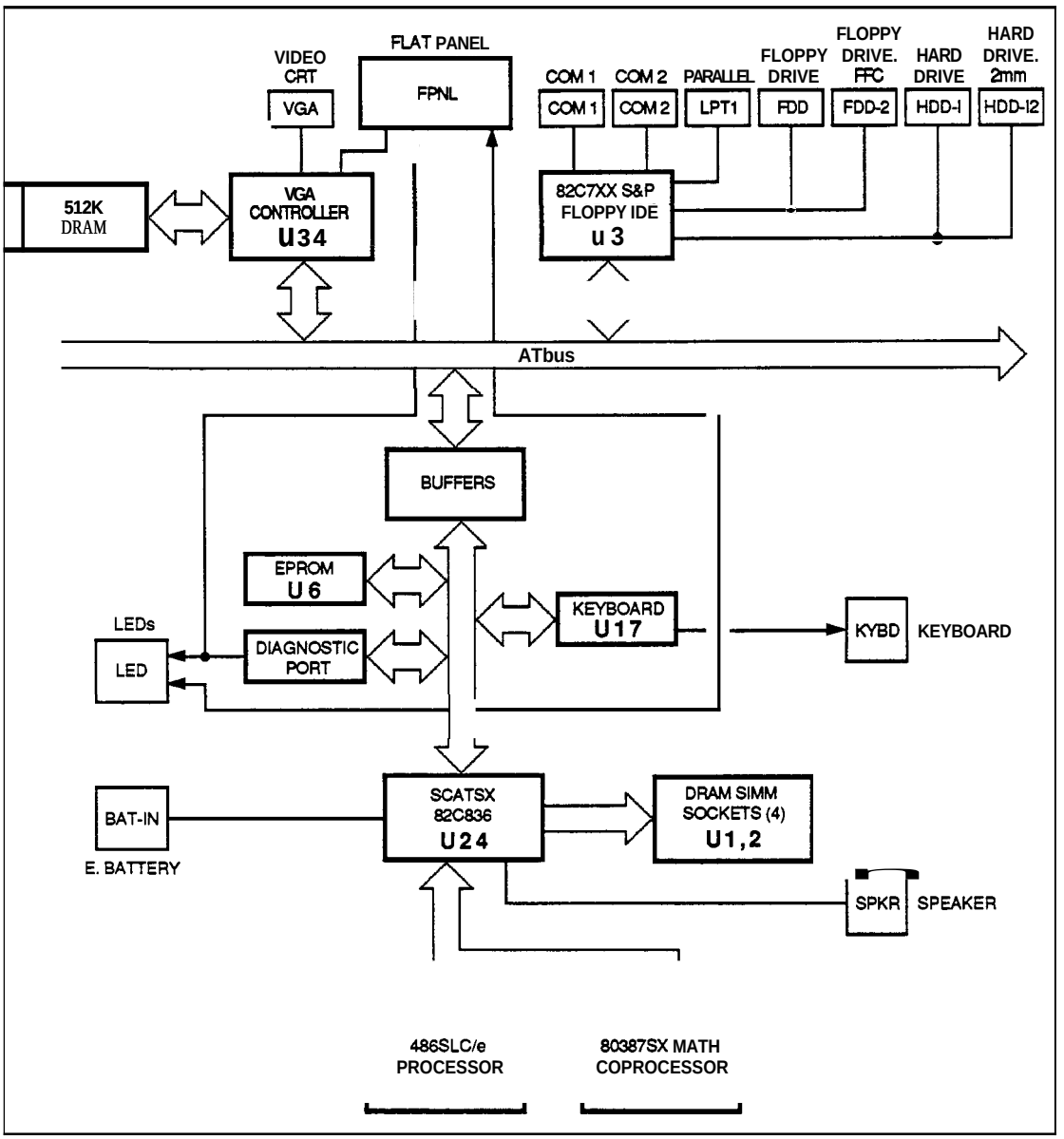


Figure 1-1. AT4SLC+ Board Block Diagram

1.4 CPU

Features of the 486SLC are highlighted below:

- Full 32-bit internal architecture
  - -8-, 16-, 32-bit data types
  - -Eight general purpose 32-bit registers
- Runs Intel 486 software in a cost-effective 16-bit hardware environment
  - -Object code compatible with 8086, 80186, 80286, and 80386 processors
  - -Runs MS-DOS, OS/2, and UNIX
- High performance 16-bit data bus with 25 MHz clock
- Integrated Memory Management Unit (MMU)
  - -Virtual memory support
  - -Optional on-chip paging
  - -Four levels of hardware-enforced protection
- Virtual 8086 mode allows executing 8086 Software in a protected and paged system
  - -Large uniform address space
  - -16 Mbyte physical
  - -64 Terabyte virtual
  - -4 Gigabyte maximum segment size
- High-speed numeric support with the 80387SX Co-processor
- On-chip debugging support including breakpoint registers
- 486-compatible instruction set
- On-chip 1 Kbyte instruction/data cache
- Highly optimized variable length pipeline and on-chip 16-bit hardware multiplier

1.5 AT CHIPSET

The 82C836 AT chipset—located at site U24—provides the following features:

- 486SLC control logic and clocks to support CPU speeds of up to 25 MHz with zero (or one) wait states.
- A 146818-compatible real time clock with 114 bytes of CMOS RAM
- Two 8237-compatible DMA controllers
- Two 8259-compatible interrupt controllers
- An 8254-compatible programmable interval timer
- An 82284-compatible clock generation and READY interface
- An 82288-compatible bus controller
- A DRAM controller that supports up to 16 Mbytes of DRAM
- A memory controller that provides shadow RAM and support for either 8-bit or 16-bit BIOS ROM
- A DRAM refresh controller

- Four EMS page register (LIM EMS 4.0 and 3.2 compatible)
- Interface logic for an 80387SX numeric co-processor
- Interface logic for an 8042 keyboard controller
- Fast Gate A20 and Fast CPU Reset logic
- Compact packaging in a single 160-pin plastic flat pack (160PQFP)

1.6 VGA CONTROLLER

The VGA controller supports all IBM VGA, EGA, CGA, and MDA modes to the register level. The VGA adapter contains 512K DRAM and supports Super VGA up to 1024 x 768 by 16 colors. The 8-bit VGA BIOS can be optionally shadowed, which increases video performance.

The VGA controller supports IBM modes 0-13h. In addition to these standard IBM modes, the following Super VGA resolutions are supported:

132 x 25 text
132 x 50 text
800 x 600 x 16 colors
800 x 600 x 16 colors
1024 x 678 x 16 colors
640 x 400 x 256 colors
640 x 480 x 256 colors
800 x 600 x 256 colors

A jumper is provided to disable the VGA (refer to Table 2-1). This allows other video adapters to be used.

1.7 I/O CONTROLLER

The I/O controller provides the system's serial, parallel, floppy, and IDE ports.

2.1 BOARD LAYOUT

This chapter provides the information necessary to configure the AT4SLC+. Figure 2-1, on the following page, illustrates the layout of the board.

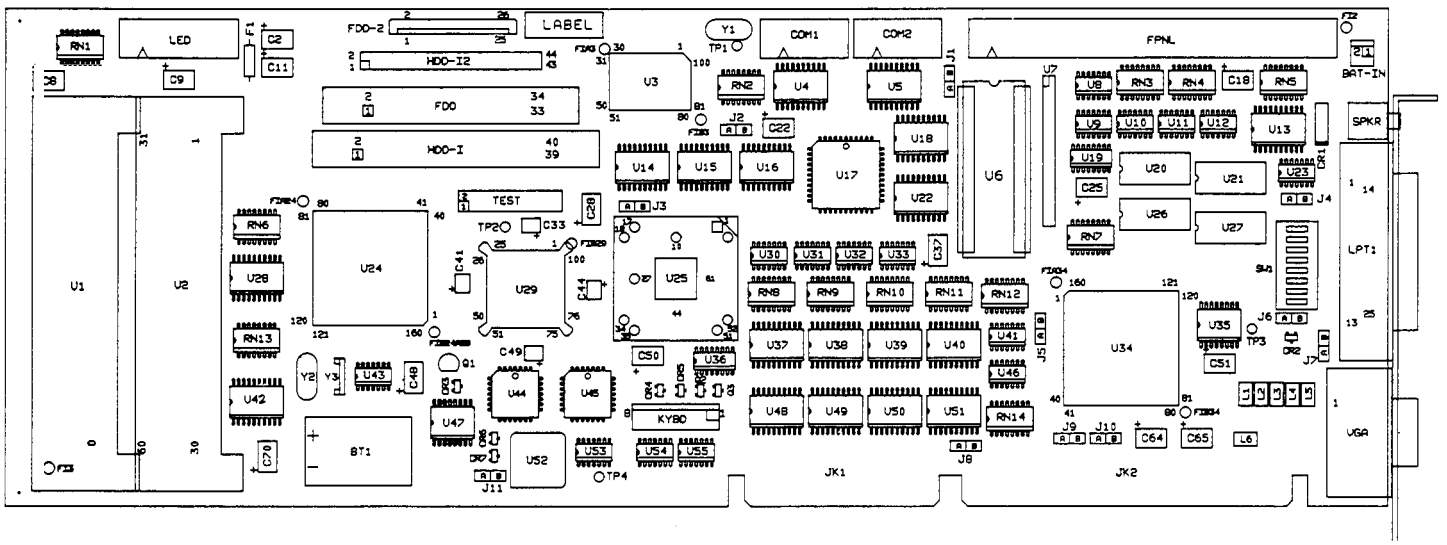


Figure 2-1. AT4SLC+ Board Layout

Figure 2-2 shows where the jumpers, connectors, and switches are located on the AT4SLC+.

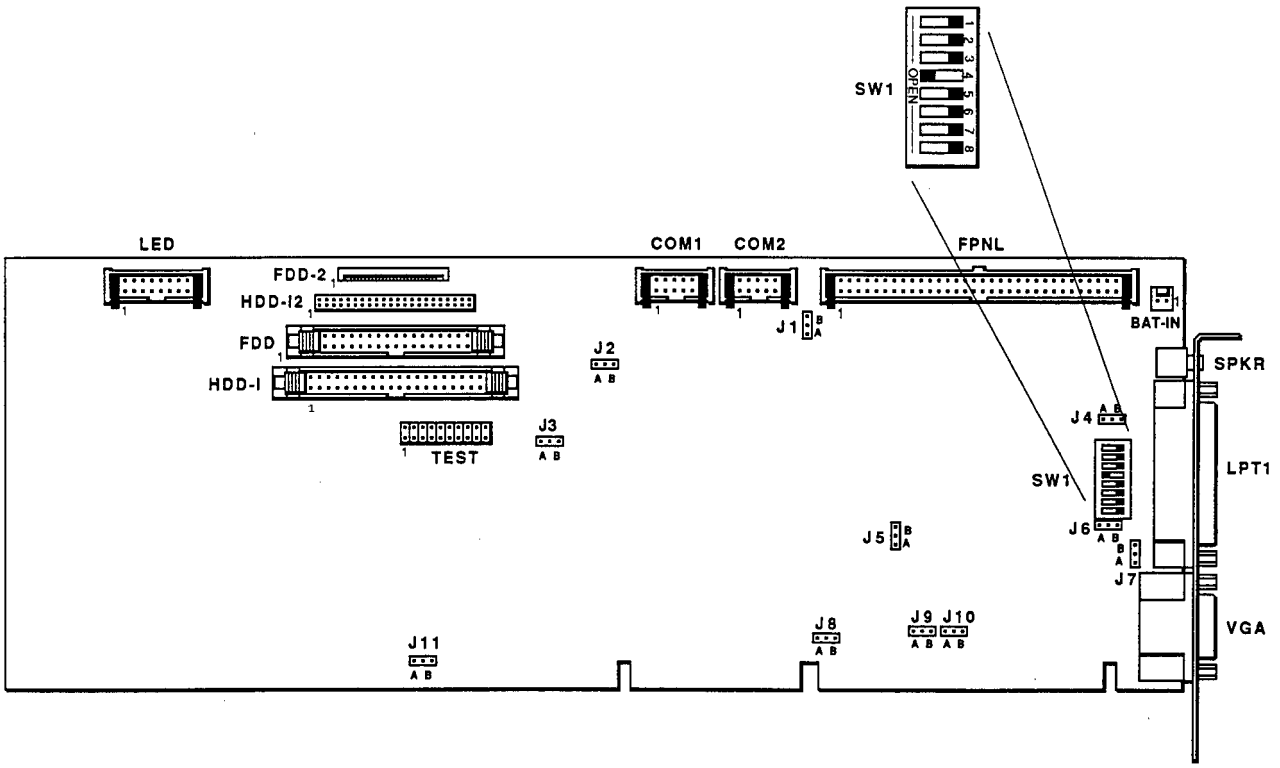


Figure **2-2.** AT4SLC+ Jumpers, Connectors, and Switches

2.2 JUMPER SETTINGS

Table 2-1 lists the AT4SLC+ jumpers, their default positions, and their functions (as illustrated in Figure 2-2).

Jumper	Position	Function
J1	***AJ***	EPROM BIOS chip
	B	Flash BIOS chip
J2	***AJ***	82C7xx chip enabled (I/O controller)
	B	82C7xx chip disabled
53	***AJ***	Secondary COM port set for IRQ3 (COM2)
	B	Secondary COM port set for IRQ11 (COM4)
54	A✓	Normal flat panel SHFCLK signal
	B	Inverted flat panel SHFCLK signal
J5	A J	VGA enabled
	B	VGA disabled
J6	A J	Battery connected by SW1-1 only
	B	Battery always installed
J7	A	Orb not connected to logic GND
	B J	Orb connected to logic GND
J8	***AJ***	Primary COM port set for IRQ4 (COM1)
	B	Primary COM port set for IRQ10 (COM3)
J9	A J	Parallel port set for IRQ7 (LPT1)
	B	Parallel port set for IRQ5 (LPT2)
J10	***AJ***	CPU does not respond to AT bus 0WS* signal
	B	CPU responds to AT bus 0WS* signal
J11	A J	Oscillator enabled
	B	Oscillator disabled

J indicates the default settings

*Zero wait state (default shipping position)

2.2.1 Disabling Functional **Blocks**

The **VGA** controller can be disabled using jumper J5 (refer to Table 2-1). The IDE and floppy drives and the parallel and COM ports can be disabled through the BIOS Setup Menus (refer to sections 4.2.1.7, 4.2.1.8, 4.2.1.15, and 4.2.1.16). You can also disable the I/O controller by changing J2 from **A** to B.

2.2.2 **Battery-Backed RAM and Real-time Clock**

> **WARNING**
> If the battery is disabled, the module must be powered up for a minimum of 30 seconds when it is re-enabled. Failure to follow this procedure may result in premature battery failure.

Jumper J6 and switch SW1-1 determine whether the on-board battery is connected to the CMOS RAM and real-time clock. When J6 is set to B or SW1-1 is closed, the battery is connected. If the settings are otherwise, the battery is disconnected. "**A**" and closed are the default settings for J6 and SW1-1, respectively. Refer to tables 2-1 and 2-2 for more information.

2.3 SWITCH OPTIONS

Table 2-2 lists the available switch options and their default settings for the AT4SLC+

Table 2-2. Switch Options

SW1-1	Open ClosedJ	When J6 is A, then battery is disconnected Battery is always connected
SW1-2	Open ClosedJ	Unused Unused
SW1-3	Open Closed✓	Monochrome display Color display
SW1-4	Open✓ Closed	Keyboard unlocked Keyboard locked
SW1-5	Open ClosedJ	FPSEL3=1 FPSEL3=0
SW1-6	Open ClosedJ	FPSEL2=1 FPSEL2=0
SW1-7	Open ClosedJ	FPSEL1=1 FPSEL1=0
SW1-8	Open ClosedJ	FPSELO=1 FPSELO=0

Jindicates the default settings

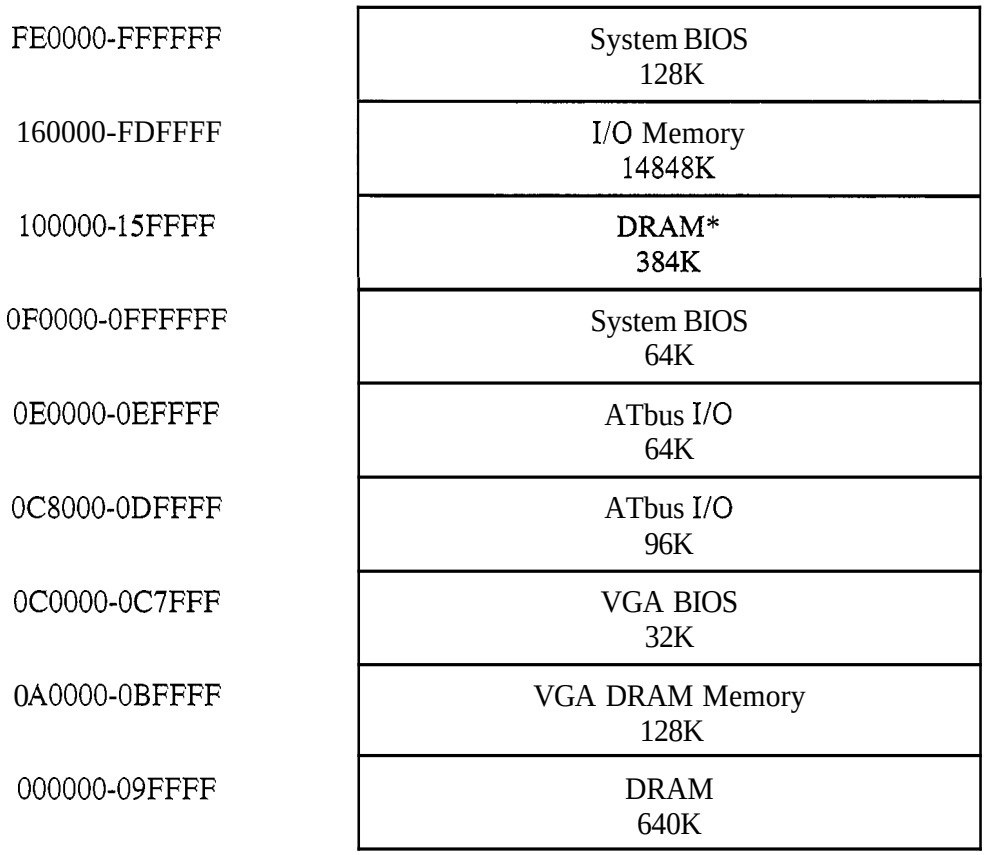
Table 2-3 lists the flat panels supported and their associated switch settings. It also lists the switch settings reserved for future flat panel types.

Table 2-3. Flat Panels Supported

SW1-5	SW1-6	SW1-7	SW1-8	Flat Panel Type
Closed	Closed	Closed	Closed	CRT
Closed	Closed	Closed	Open	Monochrome
Closed	Closed	Open	Closed	Color STN (passive)
Closed	Closed	Open	Open	Color TFT (active)
Closed	Open	Closed	Closed	Reserved
Closed	Open	Closed	Open	Reserved
Closed	Open	Open	Closed	Reserved
Closed	Open	Open	Open	Reserved
Open	Closed	Closed	Closed	Reserved
Open	Closed	Closed	Open	Reserved
Open	Closed	Open	Closed	Reserved
Open	Closed	Open	Open	Reserved
Open	Open	Closed	Closed	Reserved
Open	Open	Closed	Open	Reserved
Open	Open	Open	Closed	Reserved
Open	Open	Open	Open	Reserved

2.4 MEMORY MAPS

The AT4SLC+ has 1, 2, 4, 10, and 16 Mbyte memory maps, one for each of the five possible local memory configurations.



*The 384K of Extended DRAM is only available when no BIOS is shadowed.

Figure 2-3 1 Mbyte Memory Map (as seen by the 486SLC CPU)

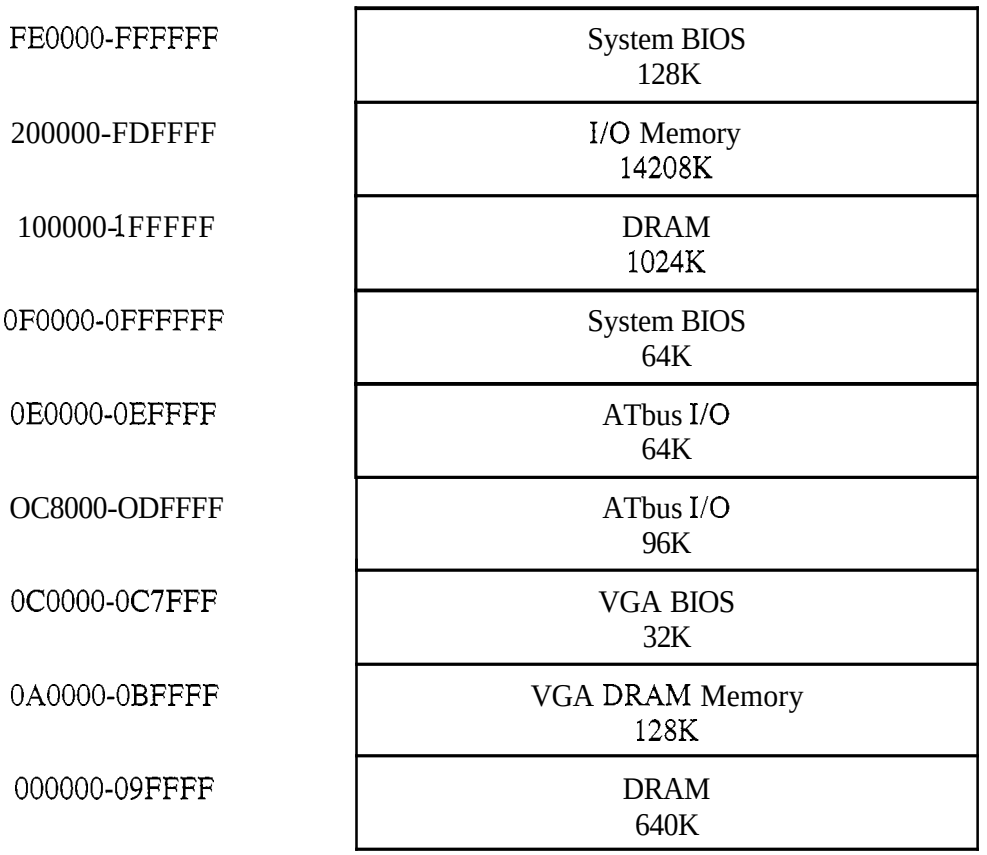


Figure 2-4. 2 Mbyte Memory Map (as seen by the 486SLC CPU)

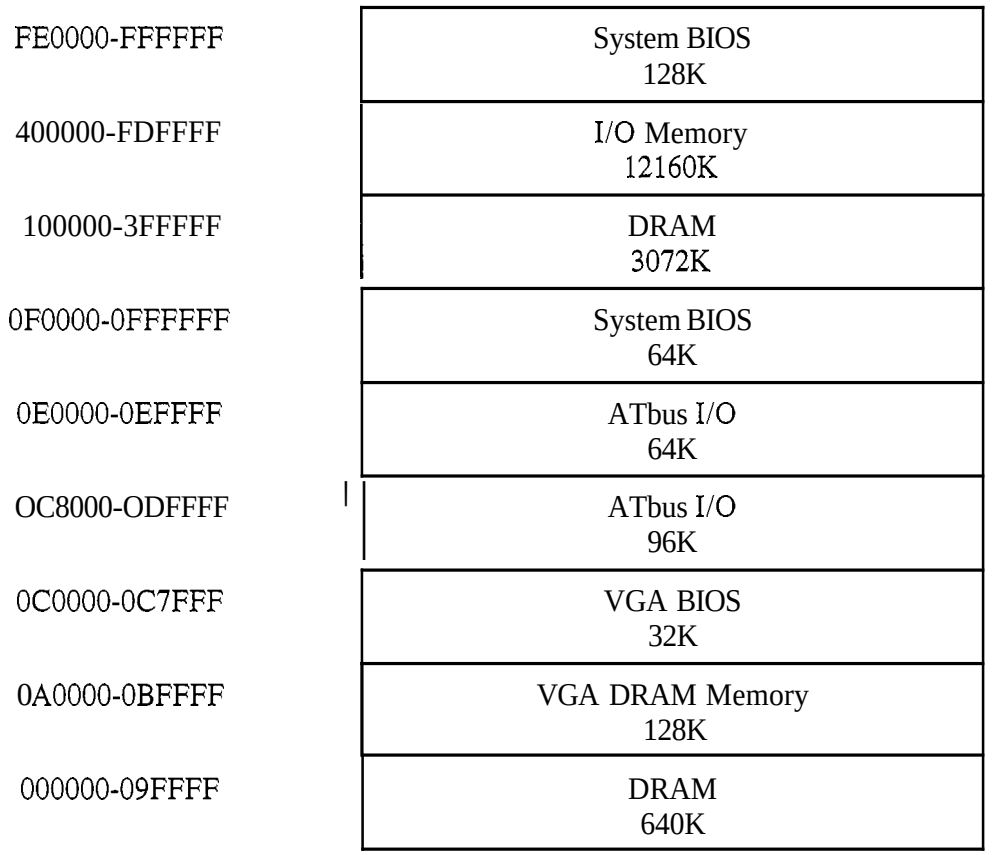


Figure 2-5. 4 Mbyte Memory Map (as seen by the 486SLC CPU)

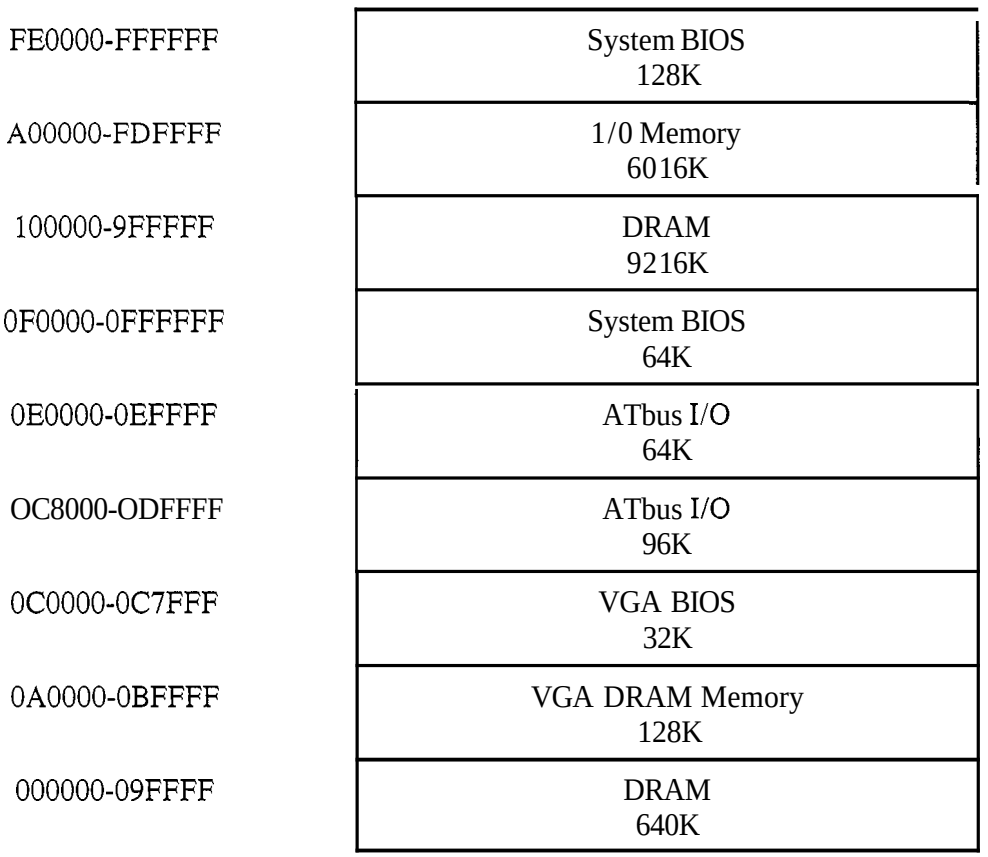


Figure 2-6. 10 Mbyte Memory Map (as seen by the 486SLC CPU)

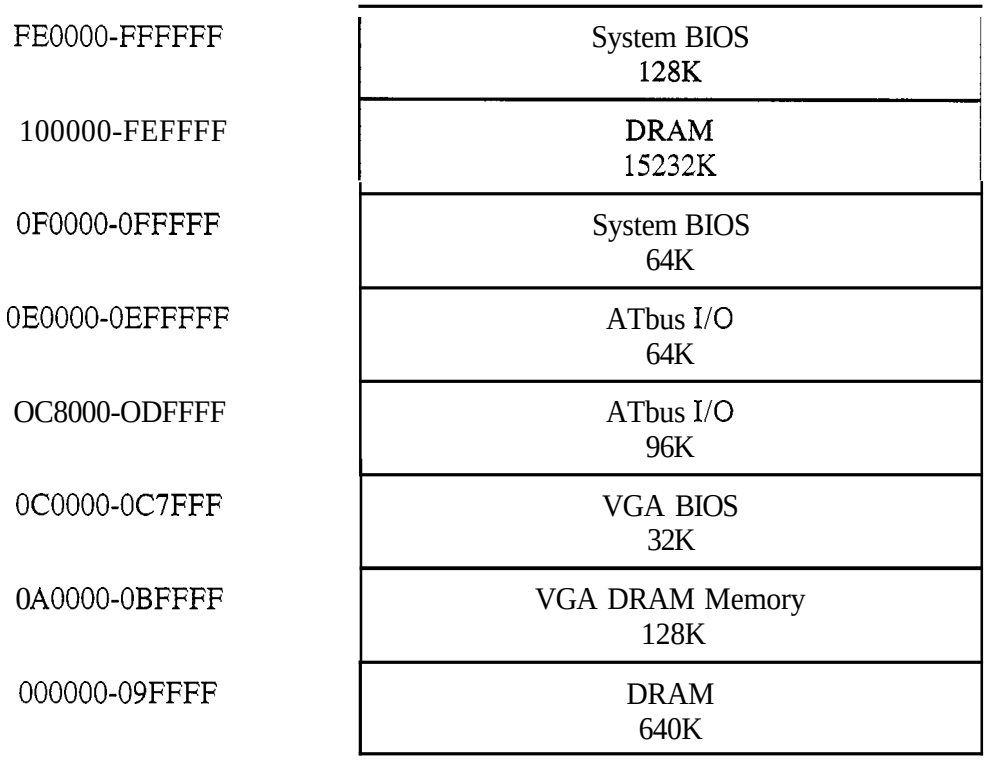


Figure 2-7. 16 Mbyte Memory Map (as seen by the 486SLC CPU)

2.5 I/O PORT ADDRESSES

The AT4SLC+ I/O map contains all IBM PC/AT architecture I/O ports, plus one I/O port at I/O address 231H. The AT4SLC+ is shipped with serial ports 1 and 2 and parallel port 1 enabled at the address specified. Standard PC/AT I/O addresses are shown in Table 2-4. Status/LED port bits are described in Table 2-5, and CMOS RAM addresses are listed in Table 2-6.

Table 2-4. I/O Address Map

Hex Range	Device
000-01F	DMA Controller 1, 8237A-5 Equivalent
020-021	Interrupt Controller 1, 8259 Equivalent
022-023	Chips & Technology Register Set-up
024-02F	Interrupt Controller 1, 8259 Equivalent
040-05F	Timer, 8254-2 Equivalent
060-06F	8742 Equivalent (Keyboard)
070-07F	Real Time Clock bit 7 NMI Mask
080-09F	DMA Page Resistor
OAO-OBF	Interrupt Controller 2, 8259 Equivalent
OCO-ODF	DMA Controller 2, 8237A-5 Equivalent
OEO-OEF	Available
0F0	Clear Math Co-processor Interrupt 13
OF1	N/A
OF2-OFF	Math Co-processor
100-1EF	Available
1FO-1F7	IDE Controller (AT drive)
1F8-277	Available
231H	Xycom LED/Status Port
278-27F	Parallel Port 2 (see note)
280-2F7	Available
2F8-2FF	Serial Port 2 (see note)
300-36F	Available
370-377	Alternate Floppy Disk Controller (see note)
378-37F	Parallel Port 1 (see note)
380-3BF	Available
3CO-3CF	VGA/EGA
3DO-3EF	Available
3FO-3F7	Primary Floppy Disk Controller
3F8-3FF	Serial Port 1 (see note)

NOTE
Because the serial and parallel port addresses can be changed and disabled, these addresses may not be used for all applications.

Xycom enclosures feature six status LEDs. Three are wired to hardware (power, disk, and COM). The remaining three—Maintenance, Fault, and RADAR—are programmable and can be accessed through Xycom's LED/Status register, located at address 231H. Table 2-4 defines the bits in this eight-bit register.

Table 2-5. LED/Status Port (address 231H)

Bit	Read/Write	Description
0	R/W	1 = Maintenance LED is off **0J** = Maintenance LED is on
1	R	**0J** = Not used
2	R/W	1 = Fault LED is off **0J** = Fault LED is on
3	R/W	1 = RADAR LED is on **0J** = RADAR LED is off
4	**R**	0 = Not used
5	R/W	1 = Write cycles to Flash BIOS enabled **0J** = Write cycles to Flash BIOS disabled
6	R	1 = VGA controller is disabled 0 = VGA controller is enabled
7	R	1 = Battery power OK 0 = Battery power low

J indicates state after a hard reset (not after <Ctrl><Alt><Del>)

Bits 0, 2, and 3 are reserved for use with the RADAR card; bits 1 and 4 are not used; bit 5 is reserved for future use of Flash BIOS; and bits 6 and 7 reflect the status of the VGA controller and battery power, respectively.

Tle 2-6. CMOS RAM Address Map

Address	Description
00-OD	Real time clock information
OE	Diagnostic status byte
OF	Shutdown status byte
10	Diskette drive type byte - drives **A** and B
11	Reserved
12	Fixed disk type byte
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19	Disk C extended byte
1A	Disk D extended byte
1B-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-3F	Reserved
40-5F	Reserved
60-6F	Reserved €or Xycom CMOS
70-7F	Reserved

2.6 SYSTEM INTERRUPTS

Table 2-7 describes the interrupts used on the AT4SLC+.

Table 2-7. AT4SLC+ System Interrupts

Interrupt	Function
IRQ1	Keyboard controller
IRQ3	Secondary COM port (COM2)*
IRQ4	Primary COM port (COM1)*
IRQ5	Parallel port (LPT2)*
IRQ6	Floppy drive
IRQ7	Parallel port (LPT1)
IRQ8	Real-time clock
IRQ9	VGA controller
IRQ10	Primary COM port (COM3)*
IRQ11	Secondary COM port (COM4)*
IRO14	IDE hard drive interface

* Interrupt selection depends on jumper configuration. Refer to Table 2-1 for more information.

2.7 SHADOW RAM

Shadowing is the process of loading the BIOS from EPROM into DRAM after power-up. Both the System and VGA BIOS can be shadowed into DRAM to increase system performance. Because shadowing the BIOS increases system performance, the AT4SLC+ is factory-shipped with the System BIOS and Video BIOS shadowed.

On the 1 Mbyte version of the AT4SLC+, the 384 Kbytes of DRAM can be used to shadow the BIOS or can be relocated to the address above the EPROM as DRAM.

The 2, 4, 10, and 16 Mbyte versions of the AT4SLC+ always allocate 384 Kbytes of DRAM for shadowing the BIOS and/or EMS memory.

2.8 CONNECTORS

The connectors for the AT4SLC+ are described below. Pinouts for each of the connectors are listed in Appendix A.

2.8.1 Floppy Drive Connector (FDD and FDD-2)

Floppy drive connector FDD is a 34-pin header; FDD-2 is a 26-pin flat flexible connector (FFC). They are the interface and control connections for up to two floppy drives.

2.8.2 IDE Hard Drive Connectors (HDD-I and HDD-I2)

IDE hard drive connector HDD-I is a 40-pin header; HDD-I2 is a 44-pin header. They are the control connectors for any hard drive(s) interfaced with the AT4SLC+. The board can control up to two hard drives from each connector.

2.8.3 COMl Serial Port Connector (COM1)

COMl is a 10-pin dual row header. A 10-pin ribbon socket to 9-pin IDC style adapter is required. For more information, refer to the system manual.

2.8.4 COM2 Serial Port Connector (COM2)

COM2 is a 10-pin dual row header. A 10-pin ribbon socket to 9-pin IDC style adapter is required. For more information, refer to the system manual.

2.8.5 VGA Connector (VGA)

The VGA connector is a 15-pin subminiature located on the bottom right of the board.

2.8.6 Parallel Port Connector (LPT1)

The Parallel port connector, LPT1, is a 25-pin female D subminiature connector.

2.8.7 **Keyboard (KYBD)**

The keyboard signals are located on an 8-pin ramp lock connector.

2.8.8 **Speaker Jack (SPKR)**

The speaker jack is a subminiature phone jack protruding through the **ORB.**

2.8.9 **External Battery (BAT-IN)**

The external battery connector is a 2-pin ramp lock connector.

2.8.10 **Flat Panel (FPNL)**

The flat panel connector is a 64-pin dual row header.

3.1 OVERVIEW

This chapter covers the installation of an optional math co-processor and additional **DRAM.**

3.2 MATH CO-PROCESSOR

An optional math co-processor is available with the AT4SLC+. To install a 80387SX or compatible 25 MHz math co-processor, insert the chip into U25 of the AT4SLC+ processor board as shown in Figure 3-1. No jumper or switch setting changes are necessary when installing a math co-processor.

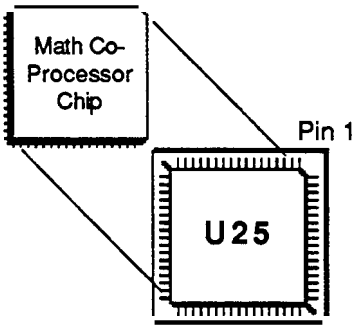


Figure 3-1. Math Co-processor Chip

3.3 DRAM

The AT4SLC+ has four single line memory modules (SIMMs) sites in which to add memory. Due to the 25 MHz CPU speed, the access time of the DRAM interface is very important. To run at 0 wait states, the SIMMs must have the following access times:

- 60ns access time for nine chip DRAM SIMMs
  or
- 70ns access time for three chip DRAM SIMMs

If you opt for 80ns DRAMs, the 0 wait state option must be changed to 1 wait state in the Setup Menu.

The AT4SLC+ can accommodate 1, 2, 4, 10, or 16 Mbytes of DRAM. SIMM sizes of 256Kx9, 1Mx9, or 4Mx9 DRAM may be used. The table below lists the combinations needed for the five memory configurations. (The "U" number location is silk screened on the back of the board.)

Memory	SIMM Site U1 (quantity)	SIMM Site U2 (quantity)
1 Mbyte	256Kx9 (2)	256Kx9 (2)
2 Mbytes	1Mx9 (2)	empty
4 Mbytes	1Mx9 (2)	1Mx9 (2)
10 Mbytes	1Mx9 (2)	4Mx9 (2)
16 Mbytes	4Mx9 (2)	4Mx9 (2)

Recommended manufacturers for DRAM, along with the respective part numbers, are listed below:

Manufacturer	1Mx9 SIMM (70NS)	256Kx9 SIMM (70NS)	4Mx9 SIMM (60NS)
Micron	MT3D19M-7	MT3D2569MP-7	N/A
Samsung	KMM591000AN-7	KMM591000AN-7	N/A
Hitachi	HB56619B-7A	N/A	HB56A49BR-6A
Xycom	98012-001	98011-001	98749-001

Figure 3-2, on the following page, shows DRAM installation.

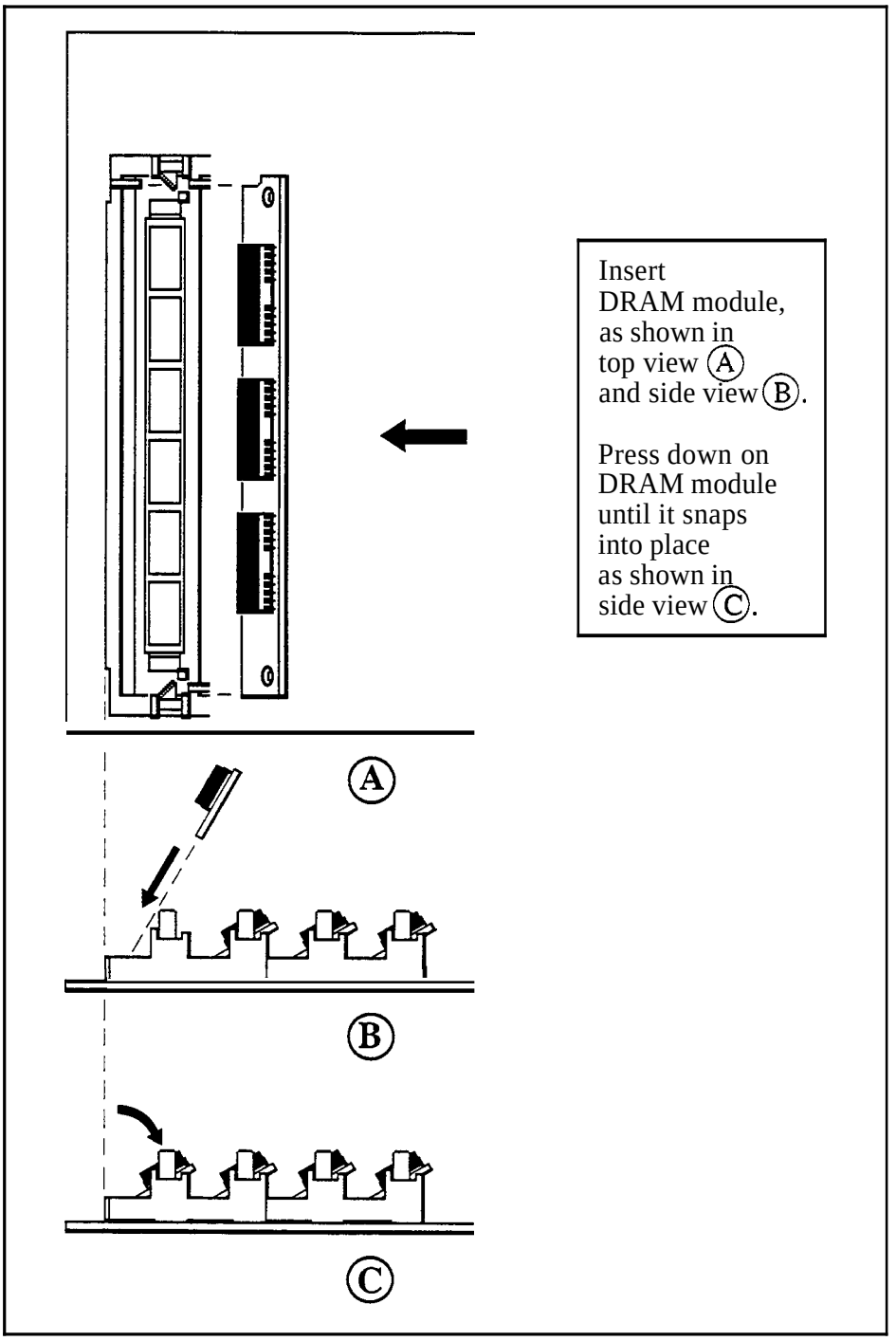


Figure **3-2.** DRAM Installation

CAUTION
Do not pull too hard on the metal tabs or the socket could snap off.

To remove a strip, pull outward on the two metal tabs on both ends of the socket. The strip should loosen in the socket and pop forward slightly for removal.

4.1 BIOS OVERVIEW

The BIOS has been customized for the AT4SLC+ board so it can surpass the functionality provided for normal PC/ATs. The custom BIOS allows users to access the value-added features present on the AT4SLC+ module without interfacing the hardware directly.

General instructions for navigating through the screens are described below:

- Arrow Keys move the cursor up, down, left, and right. Pressing <Enter> validates your selection.
- <Esc> exits the menu. You are prompted to save any changes.
- F5 selects the previous or smaller value.
- F6 selects the next or higher value.
- F9 automatically configures the system with the default values. These default values are defined by the system configuration and the values set in the Setup Menu.

> **NOTE**
> Disk drives must be configured manually

- F10 saves the current configuration. With the exception of time and date, the configuration is not saved until F10 is pressed.

4.2 BIOS MAIN SETUP MENU

The BIOS Main Setup Menu is presented as the top level in the BIOS setup menu structure. To access the Main Setup Menu, depicted below, press <Ctrl><Alt><S> simultaneously after the BIOS has completed the RAM test.

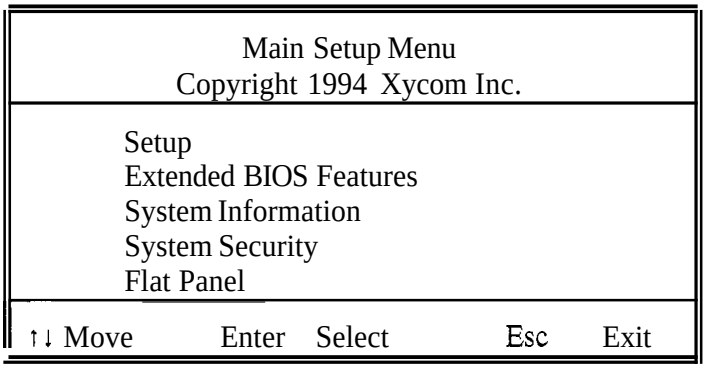


Figure 4-1. Main Setup Menu

NOTE
The Flat Panel selection in the Main Setup Menu only appears on Xycom flat panel systems.

4.2.1 **Setup Menu**

On the Setup Menu, depicted in Figure 4-2 below, the time, date, and setup information contained in the CMOS RAM can be changed. This information is used by the System BIOS for system configuration.

```
      Extended BIOS Setup - Copyright 1989-91 Quadtel Corporation

Current Date:  [01/01/1994]                Video System          [EGA/VGA]
Current Time:  [00:00:00]                  Power Up Speed        [Fast]

[     640K] System Memory                  BIOS Shadow:          [System in RAM]
[    3072K] Extended Memory                                     [Video in RAM]
       96K  Shadow Memory                   Wait States:          [0, All Banks]
      288K] EMS Memory

Internal COM A:      [COM1, 3F8h]          Internal Floppy       [Enabled      1
Internal COM B:      [COM2, 2F8h]          Internal IDE          [Enabled      1
Internal LPT:        [LPT1, 378H]          Setup Prompt          [Enabled]

Diskette Drive 0:    [1.44MB, 3 1/21       System Memory Cache   [On]
Diskette Drive 1:    [Not Installed]       AT Bus Speed          [8.33]MHz

Fixed Disk 0:  Type: [None]
Fixed Disk 1:  Type: [None]

←↑↓→  Move          F5  Previous Value     F9  Automatic Configuration
F1    Help          F6  Next Value         F10 Save Configuration
Esc   Exit
```

Figure 4-2. Setup Menu

Each of the options on the Setup Menu are described on the next few pages. Default items are underlined.

4.2.1.1 **Current Date** (<u>01/01/1994</u> format)

The date entry sets the real-time clock for the month, day, and year. The left and right arrow keys and the enter key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to type zeros in front of numbers.

4.2.1.2 **Current Time** (00:00:00 format)

The time entry sets the real-time clock for hours, minutes, and seconds. During the power up sequence, the time is read from the real-time clock and saved in the BIOS system time.

The hour is calculated according to a 24-hour military clock, i.e., 00:00:00 through 23:59:59. The left and right arrow keys and the enter key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to enter the seconds or type zeros in front of numbers.

4.2.1.3 **System Memory**

This option should always indicate the size of conventional system memory as 640 Kbytes,

4.2.1.4 **Extended Memory**

This option sets the amount of extended memory in Kbyte increments. The maximum amount of extended memory is 15 Mbytes (15296 Kbytes).

4.2.1.5 **Shadow Memory**

This field displays the amount of shadow memory in use. The contents of this field are controlled by BIOS shadow selection. Shadow memory is used to copy the system and/or video BIOS into RAM to improve performance. The AT4SLC+ allocates for Shadow RAM in Kbytes, and this number will be displayed on the menu. This field, which is not editable, is for reference only.

The AT4SLC+ is shipped with the System BIOS and Video BIOS shadowed.

> **NOTE**
> Disabling the BIOS shadow option will not increase the amount of extended memory for systems with 2, 4, 10, or 16 Mbytes DRAM. However, disabling the BIOS shadow option will increase the amount of extended memory for systems with 1 Mbyte DRAM.

4.2.1.6 **EMS Memory**

This option is used to set the amount of system memory to be configured as Expanded Memory (EMS). As the amount of EMS memory increases, the amount of extended memory decreases, and vice versa.

4.2.1.7 **Internal COM A and COM B**

These selections individually set the port address that will be programmed by the BIOS for each port. There are three options:

- Off
- Default for COM A COM1 (3F8h)
- Default for COM B COM2 (2F8h)

> **NOTE**
> It is recommended that automatic configuration be used to select the COM and LPT ports. Automatic configuration selects the first logical port address that does not conflict with any other communication port in your system. If the addresses are selected manually, conflicts with other devices in the system may occur.

4.2.1.8 **Internal LPT** (Off/LPT1, 378h/LPT1, 278h/LPT1, 3BCh)

This item selects the port address to be programmed by the BIOS for the internal LPT port. There are four options:

- Off
- LPT1 at 378h
- LPT1 at 278h
- LPT1 at 3BCh

4.2.1.9 **Diskette Drives 0 and 1**

Diskette Drive 0 (Not Installed/1.44MB, 3½"/360KB, 5¼"/1.2MB, 5¼"/720KB, 3½")
Diskette Drive 1 (Not Installed/1.44MB, 3½"/360KB, 5¼"/1.2MB, 5¼"/720KB, 3%")

These fields are used to specify the types of floppy disk drives connected to the PC/AT.

4.2.1.10 **Fixed Disk Drives 0 and 1**

Fixed Disk 0 (None/1-14/16-45/User)
Fixed Disk 1 (None/1-14/16-45/User)

This selection individually configures the disk drives as one of 45 drive types, a user-defined type, or none. If the type "User" is selected, several fixed disk parameters must be specified: number of cylinders (CY), heads (HD), sectors per track (ST), landing zone cylinder (LZ), and write precompensation (WP). Consult your fixed disk drive manual for information on any of these parameters.

4.2.1.11 **Video System**

There are four video adapter choices:

- EGA/VGA (Enhanced Graphics Adapter, Video Graphics Array, or any special video adapter)
- Monochrome
- CGA 40x25
- CGA 80x25

This field should not be changed from its default—EGA/VGA. This allows video functions to be controlled by the video BIOS rather than the system BIOS.

4.2.1.12 **Power Up Speed** (Normal/Fast)

Power up speed defaults to Fast, which is 25 MHz. When Normal is specified, the CPU runs at 12.5 MHz.

4.2.1.13 **BIOS Shadow** (System in RAM/ROM, Video in RAM/ROM)

The System BIOS and the VGA BIOS may be shadowed into DRAM. Shadowing is the process of loading the BIOS from EPROM into DRAM after power up. Since the DRAM bus width is 16 bits and the EPROM is only 8 bits, opcode fetches from the DRAM significantly increase system performance.

4.2.1.14 **Wait States** (0. All Banks/1, All Banks)

This indicates the number of wait states for memory controlled by the chipset. This default is zero for all banks. See Section **3.3.**

4.2.1.15 **Internal Floppy** (Disabled/Enabled)

This selection enables or disables the internal floppy disk drive controller.

4.2.1.16 **Internal IDE** (Disabled/Enabled)

This enables or disables the internal IDE hard disk drive controller.

4.2.1.17 **Setup Prompt** (Disabled/Enabled)

When enabled, which is the default, a prompt appears upon power up telling users how to access the Setup Menus.

4.2.1.18 **System Memory Cache** (Off/On)

The system memory cache option—which refers to the 1 Kbyte internal cache on the 486SLC—can be enabled or disabled by changing the field to On or Off. If the cache is disabled (Off), the AT4SLC+ will take longer to perform memory accesses, thereby degrading system performance.

4.2.1.19 **AT Bus Speed** (8.33 MHz/10.0 MHz)

The AT bus speed is software selectable on power up. Bus speed can be 8.33 MHz or 10 MHz.

4.2.2 **Extended BIOS Features Menu**

The Extended BIOS Features Menu is depicted below.

```
        Extended BIOS Features, Copyright 1989-91, Quadtel Corp.

Auto-park Disk:  [No  ]          Keyboard Click:      [No      ]
Quick Boot:      [No  ]          Keyboard Delay:      [3/4 Sec ]
Screen Saver:    [Disabled]      Keyboard Rate:       [22/Sec  ]
                                 Numlock Boot State:  [Off     ]

←↑↓→ Move      F5  Previous Value      F9   Auto Configuration
Esc  Exit      F6  Next Value          F10  Save Configuration
```

Figure **4-3.** Extended BIOS Features Menu

Each of the menu choices are defined below.

4.2.2.1 **Auto Park Disk** (No/Yes)

This selection determines whether the system BIOS automatically parks the fixed disk drive. If this option is enabled, the system BIOS parks the fixed disk drive(s) heads after several seconds of inactivity. Most modern hard disk drives have self-parking heads, so enabling this option may not be necessary.

> **CAUTION**
> This feature can be incompatible with fixed disk drives that are not BIOS compatible and could cause problems with programs that do not utilize the BIOS for fixed disk I/O.

> **NOTE**
> Parking the heads causes some drives to spin down so that they do not respond to accesses quickly enough and display the message: "Not ready reading drive C. Abort, Retry, Fail?"

4.2.2.2 **Quick Boot** (No/Yes)

When Quick Boot is selected, the system BIOS bypasses the floppy disk drive tests, memory tests, and floppy disk drive boot on power up or soft reset. The system initializes and boots from the fixed disk in a few seconds.

> **CAUTION**
> During hard disk partitioning and formatting, the quick boot selection must be set to No. Otherwise, an operating system missing error is displayed, and the system does not boot.

> **NOTE**
> If yes is the option selected, memory is not tested and the floppy disk drive(s) defined in the Setup Menu must be correct. Also, the system will not boot from drive **A.**

4.2.2.3 **Screen Saver** (Disabled/10 min/30 min/1 hour)

This option allows blanking the screen after a specified period of keyboard inactivity. This ensures that the data displayed does not permanently burn into the monitor. Blanking can be set to occur after 10 minutes, 30 minutes, or one hour, or this option can be disabled. Press any key to redisplay the screen after the screen saver has been activated.

> **CAUTION**
> Do **not** enable the screen saver when running programs that do not use the BIOS for keyboard handling, such as Microsoft Windows. If the screen saver is enabled with these programs, the screen blanks after the specified time, regardless of activity, and can only be restored by exiting the program.

4.2.2.4 **Keyboard Click** (No/Yes)

If enabled, this function provides audible key press feedback by causing the BIOS to click through the system speaker every time a key is pressed. This option is only valid for systems with a speaker connected to the speaker jack (SPKR).

4.2.2.5 **Keyboard Delay** (1/4, 1/2, 3/4, 1 second)

This sets the amount of time that elapses after a key is pressed before the key starts to repeat. The smaller the time selected, the sooner the key starts to repeat.

4.2.2.6 **Keyboard Rate** (2/6/10/13/18/22/27/30 per second)

This option defines the rate at which the keyboard repeats while a key is pressed. The higher the number, the faster the key repeats.

4.2.2.7 **Numlock Boot State** (Auto/On/Off)

This option determines how the BIOS defines the numlock key at power up or soft reset. Default is Off. If Auto is selected, the BIOS sets the numlock (numeric keys selected) if it detects a 101- or 102-key keyboard at power up. If an 84-key keyboard is detected, numlock is turned off (cursor keys selected). Choosing On will select the numeric keys, regardless of keyboard; Choosing Off (or leaving it as the default) will select the cursor keys, regardless of keyboard.

4.2.3 **System Information Menu**

The System Information Menu displays data about your system configuration and is shown in Figure 4-4 below. This menu is not user configurable.

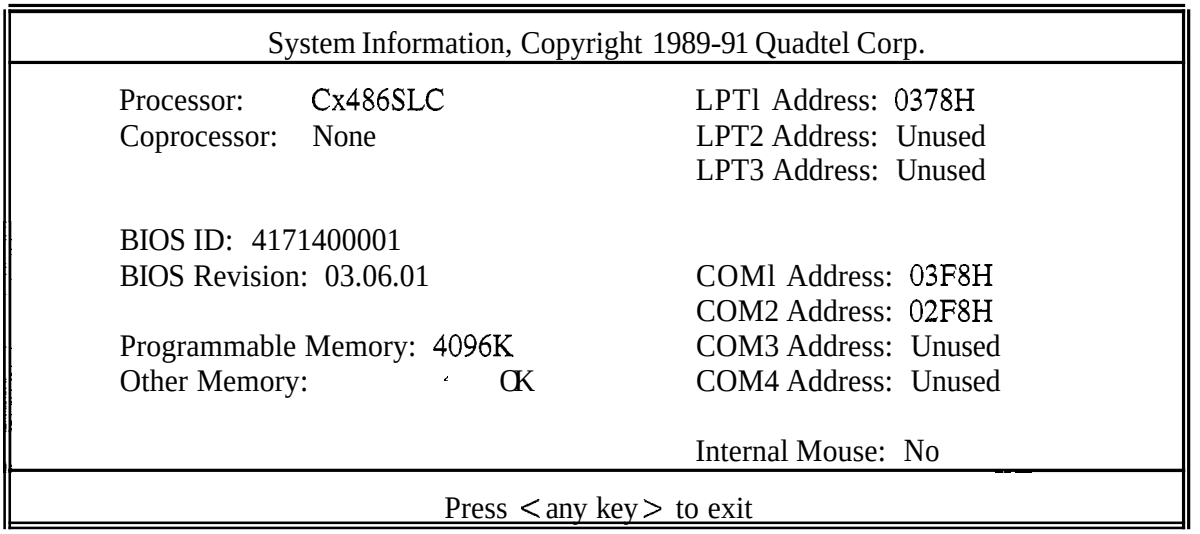


Figure 4-4. System Information Menu

The System Information Menu states the type of processor and math co-processor used, and the port addresses. The BIOS ID and revision are specific to your unit. Programmable memory is the memory controlled by the BIOS. Other memory includes ATbus memory that is annexed as DOS memory.

4.2.4 System Security

System security is provided to restrict access to your computer system. If you want to use system security, select this option and the following window will be displayed:

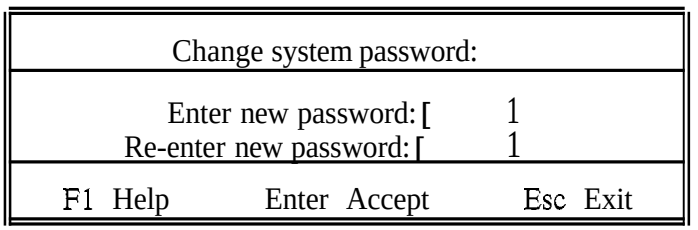


Figure **4-5.** System Security Window

Use a password value which is easy for you to remember. You may designate up to eight characters for your password (the characters are not case sensitive.). To set the password, enter the password twice. For information on what to do if you lose your password, consult the section on the next page. To remove your password, simply press <Enter> twice without entering any password characters.

Once a valid password has been entered, the BIOS will request the password each time the system is powered on or soft reset.

You must enter the same sequence of digits you entered to set the password. The BIOS will also request the password before you can enter the Main Setup Menu. This prevents unauthorized access to the system security control.

If you enter an incorrect password, the following window will display:

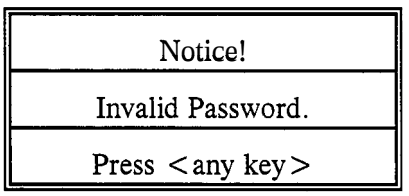


Figure 4-6. Incorrect Password Window

After entering an incorrect password three times, the following window will display:

```
!! SYSTEM DISABLED !!
(013AD8)
```

Figure 4-7. System Disabled Window

If this window appears, the system has been halted. Reset the system and enter the corre passw rd.

If you lose your password, write down the number in parentheses on the System Disabled Window and contact Xycom. Using this number, we can generate an alternate password that will allow you to gain access to your system.

4.2.5 **Flat Panel Menu**

If you select the Flat Panel entry in the Main Setup Menu (this selection will only appear on a Xycom flat panel system), a menu will appear only if a flat panel display is connected. If the flat panel does not support backlight blanking, "Not Available" will be in the timeout field. In a system that has a flat panel that allows backlight blanking, the menu shown below will allow you to disable backlight blanking, or set the backlight timeout.

```
Flat Panel Menu, Copyright 1994, Xycom Inc.

Backlight Blanking Timeout: [10 minutes]

↑↓ Move          F5 Previous Value
Esc Exit         F6 Next Value          F10 Save Configuration
```

Figure 4-8. Flat Panel Menu

When blanking is enabled, the flat panel backlight will be turned off if no keys are pressed within the specified time. The blanking timeout can be set to any multiple of five minutes up to a maximum of 60 minutes. After the backlight has been turned off, pressing any keyboard or keypad key will turn the backlight back on. (The keycode of the key that was pressed to turn on the backlight will not be passed to the software currently running on the system.)

4.3 BIOS COMPATIBILITY

This BIOS is IBM PC/AT compatible with additional CMOS RAM and BIOS data areas used.

4.3.1 CMOS RAM Usage

This BIOS uses the standard PC/AT battery-backed CMOS RAM. Xycom reserves addresses 60H-6EH in addition to the standard BIOS definitions.

4.3.2 BIOS Data Area Usage

This BIOS uses the standard PC/AT BIOS data area locations, as well as the following locations: 0040H:00F0H, 0040H:00F2H, and 0040H:00F4H.

4.3.3 POST Codes

Xycom provides Power On Self Test (POST) codes for this BIOS in addition to those provided by Quadtel. If you use a POST board for testing, call Xycom for a current list of these codes.

This appendix describes the pinouts for the AT4SLC+ connectors defined in Chapter 4.

A.1 FLOPPY DRIVE CONNECTOR (FDD and FDD-2)

Floppy drive connector FDD is a 34-pin header; FDD-2 is a 26-pin flat flexible connector (FFC). They are the interface and control connections for up to two floppy drives.

Table A-1. Floppy Drive Connector (FDD)

PIN	SIGNAL	PIN	SIGNAL
1	GND	18	FDIRC*
2	FRWC*	19	GND
3	GND	20	FSTEP*
4	N/C	21	GND
5	KEY	22	FWD*
6	N/C	23	GND
7	GND	24	FWE*
8	IDX*	25	GND
9	GND	26	FTK0*
10	MO1*	27	GND
11	GND	28	FWP*
12	FDS2*	29	GND
13	GND	30	FRDD*
14	FDS1*	31	GND
15	GND	32	FHS*
16	MO2*	33	GND
17	GND	34	DCHG*

Table A-2. Floppy Drive Connector (FDD-2)

Pin	**Signal**	Pin	**Signal**
1	+5V	14	FSTEP*
2	IDX*	15	GND
3	+5V	16	FWD*
4	FDS1*	17	GND
5	+5V	18	FWE*
6	DCHG*	19	GND
7	N/C	20	FTKO*
8	N/C	21	GND
9	N/C	22	FWP*
10	MO1*	23	GND
11	N/C	24	FRDD*
12	FDIRC*	25	GND
13	GND	26	FHS*

A.2 **IDE** HARD **DRIVE CONNECTORS (HDD-I and HDD-I2)**

IDE hard drive connector HDD-I is a 40-pin header; HDD-I2 is a 44-pin header. They are the control connectors for any hard drive(s) interfaced with the AT4SLC+. The board can control **up** to two hard drives from each connector.

Table A-3. IDE Hard Drive Connector (HDD-I)

Pin	Signal	Pin	Signal
1	RESET*	21	N/C
2	GND	22	GND
3	IDED7	23	IOW*
4	SD8	24	GND
5	SD6	25	IOR*
6	SD9	26	GND
7	SD5	27	N/C
8	SDlO	28	ALE
9	SD4	29	N/C
10	SD11	30	GND
11	SD3	31	IRQ14
12	SD12	32	IOCS16*
13	SD2	33	SA1
14	SD13	34	N/C
15	SD1	35	SA0
16	SD14	36	SA2
17	SDO	37	HCS0*
18	SD15	38	HCS1*
19	GND	39	HDACTIVE*
20	N/C	40	GND

Table A-4. IDE Hard Drive Connector (HDD-I2)

Pin	Signal	Pin	Signal
1	RESET*	23	IOW*
2	GND	24	GND
3	IDB7	25	IOR*
4	SD8	26	GND
5	SD6	27	N/C
6	SD9	28	ALE
7	SD5	29	N/C
8	SDlO	30	GND
9	SD4	31	IDEINT
10	SD11	32	ATIOCS16*
11	SD3	33	SA1
12	SD12	34	N/C
13	SD2	35	SA0
14	SD13	36	SA2
15	SD1	37	HCS0*
16	SD14	38	HCS1*
17	SDO	39	HDACTIVE*
18	SD15	40	GND
19	GND	41	+5v
20	N/C	42	+5v
21	N/C	43	GND
22	GND	44	N/C

A.3 COMl SERIAL PORT CONNECTOR (COM1)

COMl is a 10-pin dual row header. **A** 10-pin ribbon socket to 9-pin IDC style adapter is required.

Pin	Signal	Pin	Signal
1	DCD1	6	CTS1
2	DSR1	7	DTR1
3	RXD1	8	RI1
4	RTS1	9	GND
5	TXD1	10	NO CONNECT

COM2 is a 10-pin dual row header. **A** 10-pin ribbon socket to 9-pin IDC style adapter is required.

Table **A-6.** COM2 Serial Port Connector

Pin	Signal	Pin	Signal
1	DCD2	6	CTS2
2	DSR2	7	DTR2
3	RXD2	8	RI2
4	RTS2	9	GND
5	TXD2	10	NO CONNECT

A.5 VGA CONNECTOR (VGA)

The VGA connector is a 15-pin subminiature located on the bottom right of the board.

Table A-7. VGA Connector

Pin	Signal	Pin	Signal
1	RED	9	KEY
2	GREEN	10	GND
3	BLUE	11	N/C
4	N/C	12	N/C
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	N/C
8	GND		

A.6 PARALLEL PORT CONNECTOR (LPT1)

The Parallel port connector, LPT1, is a 25-pin female D subminiature connector

Table A-8. Parallel Port Connector

Pin	Signal	Pin	Signal
1	STROBE	14	AUTOFEED
2	PDO	15	PERROR
3	PD1	16	INIT
4	PD2	17	SELIN
5	PD3	18	GND
6	PD4	19	GND
7	PD5	20	GND
8	PD6	21	GND
9	PD7	22	GND
10	PACK	23	GND
11	PBUSY	24	GND
12	PE	25	GND
13	SELECT		

A.7 KEYBOARD (KYBD)

The keyboard signals are located on an 8-pin ramp lock connector

Table A-9. Keyboard Connector

Pin	Signal
1	SPEAKER
2	+5v
3	KBINHIBIT*
4	DATA
5	CLK
6	NC
7	GND
8	NC

A.8 SPEAKER JACK (SPKR)

The speaker jack is a subminiature phone jack protruding through the ORB.

Table A-10. Speaker Jack

Pin	Signal
TIP	SOURCES CURRENT
SLEEVE	GND

A.9 EXTERNAL BATTERY (BAT-IN)

The external battery connector is a 2-pin ramp lock connector.

Table A-11. External Battery Connector

Pin	Signal
1	BATTERY -
2	BATTERY +

A.10 FLAT PANEL CONNECTOR (FPNL)

The flat panel connector is a 64-pin dual row header.

Table **A-12.** Flat Panel Connector

Pin	Signal	Pin	Signal
1	GND	33	GND
2	MAINT LED	34	FP11
3	FAULT LED	35	GND
4	SERIAL LED	36	BLANK
5	DRIVE LED	37	GND
6	RADAR LED	38	SHFCLK
7	GND	39	GND
8	KB CLOCK	40	LP
9	GND	41	GND
10	RESET*	42	FLM
11	GND	43	GND
12	ENAVDD*	44	ACDCLK
13	GND	45	GND
14	ENAVEE*	46	FP17
15	GND	47	FP18
16	FPO	48	FP19
17	FP1	49	FP20
18	FP2	50	GND
19	FP3	51	FP21
20	GND	52	FP22
21	FP4	53	FP23

Table continued on the following page.

Table **A-12.** Flat Panel Connector *(continued)*

Pin	Signal	Pin	Signal
22	FP5	54	FP24
23	FP6	55	GND
24	FP7	56	N/C
25	GND	57	N/C
26	FP8	58	N/C
27	GND	59	N/C
28	FP9	60	N/C
29	GND	61	N/C
30	FP10	62	N/C
31	GND	63	N/C
32	FP11	64	GND

Numerical

A

B

C

D

E

F

I